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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,621	06/08/2000	Salman Akram	3936US (99-0066)	1302

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EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	25

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/590,621	AKRAM ET AL.
	Examiner	Art Unit
	Nema O Berezny	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 36-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-23 and 41-49* is/are allowed.

6)☒ Claim(s) *1-6,8-17 and 36-40* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *19* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4-3-03 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 10-12, 14-16, 36, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe (JP 58-157146). Watanabe discloses a method of modifying a semiconductor die, comprising: providing at least one semiconductor die (Figs.1-2 el.1) having an active surface; and forming on or securing to said active surface at least one stabilizer (el.6) comprising a dielectric material (Constitution) such that said at least one stabilizer protrudes from said active surface, said stabilizer being configured to space said at least one die a substantially fixed distance apart from a

higher-level substrate (el.4) when disposed active surface-down over said higher-level substrate (Fig.1). Watanabe also discloses forming a plurality of stabilizers (Fig.2); forming said stabilizers adjacent at least one corner of said active surface (Fig.2); forming at least two stabilizers adjacent opposite peripheral edges of said active surface (Fig.2); forming selected ones of said plurality of stabilizers to have a height that defines a substantially consistent die-to-substrate distance (Fig.1); forming said at least one stabilizer from photoimageable material (Constitution); adhering (implied) said stabilizer to said active surface; wherein said forming said stabilizer comprises applying a layer of insulative material or photoresist material on said active surface and patterning said layer (Constitution), and positioning said stabilizer on said active surface so as to avoid contact with conductive traces on said substrate (Fig.1; Constitution); disposing at least one conductive structure or solder bump (el.3) on at least one bond pad (el.2) of said at least one semiconductor die (el.1). Watanabe also discloses inverting and positioning said die on said substrate to contact said conductive structures to corresponding contacts, and bonding said conductive structures to the corresponding contacts (Fig.1); and wherein said forming said stabilizer comprises configuring said stabilizer to be positioned between a periphery of said surface of said die and said conductive structures (Figs.1-2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe as applied to claims 1-6 above. Watanabe does not disclose providing a semiconductor wafer including a plurality of semiconductor dice. However, It is well known in the semiconductor industry to use wafer fabrication for the purpose of cost and time savings through mass fabrication.

Claims 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe as applied to claims 1-6 and 10-12 above, and further in view of Kuniaki (JP 10189653). Watanabe does not disclose forming a sealing material between said die and said substrate. However, Kuniaki discloses introducing encapsulating material between a flip chip die and a substrate, wherein said encapsulant is securable to a stabilizer (Fig.2). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the encapsulating of Kuniaki with the method of forming a flip chip die of Watanabe in order to protect said device from environmental, chemical, and mechanical stress and contaminants.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe as applied to claims 1-6, 10-12, and 14-16 above, and further in view of Liang (5,639,696). Watanabe does not disclose applying one of a conductive pillar, a conductor filled epoxy pillar, and a structure of z-axis elastomer to said bond pad.

However, Liang discloses a conductive pillar (Fig.4 el.52) positioned on a bond pad for a flip chip device. Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the conductive pillars of Liang with the semiconductor device method of Watanabe in order to mass fabricate solder columns in a grid array structure (col.3 lines 19-25).

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe as applied to claim 36 above, and further in view of Blanton (5,220,200). Watanabe does not disclose forming a stabilizer structure to have a height less than a minimum distance said conductive structures protrude from the die active surface. However, Blanton discloses forming a stabilizer structure to have a height less than a minimum distance said conductive structures protrude from the die active surface (Fig.2). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the stabilizer structure of Blanton with the semiconductor device method of Watanabe in order to self-align the solder bumps and form consistent electrical and mechanical joints between the die and substrate (col.9 lines 4-16).

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe as applied to claim 36 above, and further in view of Ghaem (6,046,910). Watanabe does not disclose forming a stabilizer to space the surface from the substrate a distance greater than a minimum distance at least one of said conductive structures protrudes from said surface. However, Ghaem discloses a stabilizer that is spaced from

the surface of said die to said substrate, which is a greater distance than a minimum distance that said conductive structures protrude from said surface (Fig.1). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the stabilizer structure of Ghaem with the semiconductor device method of Watanabe in order to form a narrower or thinner conductive structure.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Ghaem as applied to claim 38 above, and further in view of Liang (5,639,696). Watanabe and Ghaem do not disclose forming a stabilizer structure to lengthen at least one of said conductive structures. However, Liang discloses forming a stabilizer structure to lengthen at least one of said conductive structures (Abstract). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the stabilizer structure of Liang with the semiconductor device method of Watanabe in view of Ghaem in order to form column conductive structures of a consistent height using a mass fabrication method of a grid array (col.3 lines 19-26).

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter for claims 7 and 18: the prior art of record does not disclose or teach a method of modifying a semiconductor device component, comprising: providing at least one semiconductor substrate with contact pads on an active surface thereof; and sequentially forming on said active surface at least one stabilizer having a plurality of

superimposed, contiguous, mutually adhered layers of photopolymer, said at least one stabilizer being configured to at least partially stabilize an orientation of the deivce upon being disposed active surface-down over a higher-level substrate.

Blanton (5,220,200) discloses said method, except said stabilizer is not formed by a plurality of superimposed, contiguous, mutually adhered layers of photopolymer (Fig.2; col.7 lines 7-25).

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter for claims 19-23 and 41-49: the prior art of record does not teach or disclose a method of modifying a semiconductor device component, comprising: placing at least one semiconductor substrate having an active surface with contact pads exposed thereon in a horizontal plane; recognizing a location and orientation of said at least one substrate; applying a layer of a partially uncured photopolymer to said semiconductor; stereolithographically forming on said active surface between one of said contact pads and a peripheral edge of said at least one substrate, at least one stabilizer comprising at least one layer of an electrically nonconductive semisolid material.

Blanton (5,220,200) discloses said method, except Blanton does not form said stabilizer by stereolithography (col.8 lines 27-30). Blanton also discloses that his stabilizer is formed using the same materials and methods as the normal fabrication of

the semiconductor device (col.8 lines 33-44), and therefore it would not be obvious to combine Blanton with a stereolithographic method.

Response to Arguments

Applicant's arguments with respect to claims 1-6, 8-17 and 36-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are for stereolithographic structures formed upon a semiconductor device, but said structures are not used as a stabilizer structure between a semiconductor device and a substrate. Said references are by the same assignee as the instant application and would only qualify as a 102(e) reference, and therefore cannot be combined with any other reference as a 103(a) rejection.

6,524,346 (Farnworth) – Fig.9; col.7 lines 52-65

6,529,027 (Akram et al.) – Fig.1A ; col.9 line 42 – col.10 line 34

6,531,335 (Grigg) – col.6 lines 24-62

6,549,821 (Farnworth et al.) – Abstract

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (703) 305-3445. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NB
May 5, 2003

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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